

Substitute Form PTO-1449 (Modified)  <b>Information Disclosure Statement          by Applicant</b> (Use several sheets if necessary)  (37 CFR §1.98(b))	U.S. Department of Commerce Patent and Trademark Office	Attorney's Docket No. <b>10559-132002</b>	Application No. <b>10/684,078</b>
	Applicant <b>Gilbert Wolrich et al.</b>		
	Filing Date <b>October 10, 2003</b>	Group Art Unit <b>2661</b>	

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Examiner Initial	Desig. ID	Document Number	Publication Date	Patentee	Class	Subclass	Filing Date If Appropriate
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	FJ	7,191,321	03/2007	Bernstein et al.			
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							Yes	No
	FM	0 773 648	05/1997	EPO				
	FN	WO 00/38376	06/2000	WIPO				
	FO	WO 00/56024	09/2000	WIPO				
	FP	WO 01/31856	05/2001	WIPO				

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	FR	Agarwal et al., "April: A Processor Architecture for Multiprocessing," Proceedings of the 17th Annual International Symposium on Computer Architecture, <i>IEEE</i> , pp. 104-114, (1990).
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	FT	Farrens, et al., "Strategies for Achieving Improved Processor Throughput", <i>ACM</i> , pg. 362-369 (1991).
	FU	Giroux, N., et al., "Queuing and Scheduling: Quality of Service in ATM Networks, Chapter 5", <u>Quality of Service in ATM Networks: State-of-the-Art Traffic Management</u> , pp. 96-121 (1998).
	FV	Govind, et al., "Performance modeling and architecture exploration of network processors", <i>Quantitative Evaluation of Systems</i> , abstract only (1 page), Sep. 2005.
	FW	Kaiserswerth, M., "The Parallel Protocol Engine", <i>IEEE/ACM Transactions on Networking</i> , 1(6):650-663, December 1993.
	FX	Khailany, B., et al., "Imagine: Media Processing with Streams," <i>IEEE Micro</i> , March-April 2001, pp. 35-46.

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	GE	Vuppala, V., et al., "Layer-3 switching using virtual network ports", <i>IEEE Proc. Computer Communications and Networks</i> , pp. 642-648, 1999.
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